Amendments to the Specification:

Please replace paragraph [20] with the following amended paragraph:

As in the computer system 10 of Figure 1, the system controller 110 also includes a memory hub controller 128 that is coupled to several memory modules 130a,b...n, which serve as system memory for the computer system 100. The memory modules 130 are each coupled to a first high-speed downstream bus 132 and a first high-speed upstream bus 134. The first downstream bus 132 extends downstream from the memory hub controller 128, and a second downstream bus 132 extends from each of the memory modules 130 except the memory module 130n furthest from the memory hub controller 128. Similarly, the first upstream bus 134 extends upstream from the first memory module 130a to the memory hub controller 128, and a second upstream bus 134 extends from each of the memory modules 130 to a respective upstream memory module. Each of these buses 132, 134, include a discrete data bus, although they may also include discrete command and address buses, a combined command/address bus, or some other bus system. However, the explanation of the various embodiments will be with respect to a data bus, it being understood that a similar technique can be used to strobe command and address signals.

Please replace paragraph [28] with the following amended paragraph:

One embodiment of the receivers 142, 182 and the transmitters 144, 180 in the memory hub controller 128 and in one of the memory modules 130 is shown in Figure 3. In both cases, a receiver 200 functions as both receivers 142, 148 in the memory module 130 and the receiver 182 in the memory hub controller 128, and a transmitter 210 functions as both transmitters 144, 146 in the memory module 130 as well as the single transmitter 180 in the memory hub controller 128. The transmitter 210 in the system controller 110 includes a pattern generator 220 that generates a first predetermined pattern of data bits, and a transmit interface control 224 that controls the transmitting of the pattern. In the embodiment of Figure 3, the same first predetermined data pattern is transmitted on all of the data bits of the buses 132, 134. Alternatively, the transmitter 210 in the system controller 110 can transmit a first predetermined pattern of data on the downstream bus 132, and the transmitter 210 in the memory hub 130 can

transmit a second predetermined pattern of data on the upstream bus 134 that is different from the first predetermined pattern of data.

Please replace paragraph [34] with the following amended paragraph:

One embodiment of the pattern comparator 234 is shown in Figure 4 along with the pattern generator 220 and the transmit interface controller 224 in the transmitter 210 and the expected pattern memory 230, the phase adjustment logic 240 and the receive interface controller 244 as shown in Figure 3. The pattern comparator 234 includes a set of 32 double data rate ("DDR") flip-flops 250 that receive the receive clock signal from a receive clock generator 254 and capture 32 bits of data responsive to each transition of the receive clock signal. The clock generator 254 receives a reference clock signal having a lower frequency than the receive clock signal and is operable to generate the receive clock signal from the reference clock signal. As each 32 bits of data are captured by the flip-flops 250, the 32 bits of data that were captured on the previous transition of the receive clock signal are transferred to a receive capture buffer 258. The buffer 258 is a recirculating buffer that is able to store data from 24 transitions of the receive clock signal, which occur responsive to twelve periods of the receive clock signal or three periods of the core clock signal. Thus, the buffer 258 stores 768 bits of data (*i.e.*, 24 * 32), and, since it is a recirculating buffer, the oldest data bits stored in the buffer 258 are overwritten with new data bits. The data stored in the receive capture buffer 258 are 32 bits for each of the positive edge and the negative edge of the receive clock signal. There are 12 locations in the buffer 258 that store data for the positive edge and 12 locations in the buffer 258 that store data for the negative edge. Each of these locations is 32 bits wide. The receive capture buffer 258 outputs data from 4 locations for the positive edge and 4 locations for the negative edge. As a result, 256 bits are coupled from the buffer 258, *i.e.*, 32 bits for each of 8 locations.

Please replace paragraph [35] with the following amended paragraph:

The 32 bits from the receive capture buffer 258 are applied to a multiplexer 260, which selects one of four sets of bits for coupling to a set of flip-flops 264. Each set consists of 4 bits from 4 respective locations for the positive edge and 4 bits from 4 respective locations for the negative edge. The number N of data bits in each of the sets is given by the formula:

$$N=[(f_1*m)/(f_2)]$$

where f_1 is the frequency of the receive clock signal, f_2 is the frequency of the reference clock signal, and m is the number of data bits captured by the flip-flops during each period of the receive clock signal. The first set consists of bits 0, 1, 2, 3 for both the positive and negative edges, the second set consists of bits 4, 5, 6, 7 for both the positive and negative edges, the third set consists of bits 8, 9, 10, 11 for both the positive and negative edges. One of these three sets of eight data bits are selected by a pointer register 266, which is incremented by the receive interface controller 244 in a manner that will be explained below. The flip-flops 264 are clocked by an internal core clock signal that is generated from the reference clock signal.